REMARKS

By way of this amendment and reply to the Office Action mailed August 14, 2002, claims 1, 6, 11 and 18 have been amended, and new claims 25-32 have been added. Support for new claims 25-28 may be found, for example, in Figure 13A of the drawings and in the description of that figure in the specification, and support for new claims 29-32 may be found, for example, in Figures 12A and 12B of the drawings and in the description of those figures in the specification. Claims 1-4, 6-9, 11-16 and 18-32 are presently pending for further consideration.

In the Office Action, claims 1-4, 6-9, 11-16 and 18-23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,326,270 to Lee et al. This rejection, to the extent that it may be applied to the presently pending claims, is traversed for at least the reasons given below.

In Lee et al., the second nitride film 119 serves as an etch stopping layer during the etching of the first and second interlayer insulating layers 130 and 120 to define contact holes 131a - 131e. See column 9, lines 48-51 of Lee et al. In the present invention as recited in claim 1, however, a first nitride film, which is formed beneath a second nitride film, serves as an etch stopping layer during the formation of contact holes. In the present invention, the second nitride layer prevents the impurity in the interlayer insulating film from being diffused into the semiconductor substrate when the interlayer insulating film is annealed in water vapor, as explained on page 25, lines 18-25 of the specification. Applicants disagree with the Examiner's assertion that Lee et al.'s lack of teaching of annealing steps would be a matter of obvious design choice, since Lee et al.'s use of first and second nitride layers is for a much different purpose than that of the present invention. Thus, even if Lee et al. was to be modified to include annealing steps, it is believed that one skilled in the art would not provide such annealing steps in the precise sequence as recited in independent claims 1, 6, 11 and 18, without hindsight knowledge of the claimed invention. As such, the usefulness of the second nitride layer would not be obtained by one of ordinary skill in the art.

Furthermore, independent claims 1, 6, 11 and 18 have been amended to clarify that all portions of the second nitride film that are in direct contact with the first nitride film positioned on sides of the gate electrodes are removed during the self-aligning step. This feature can be clearly seen in Figure 13A of the drawings, whereby the second nitride film 109 has been removed from the portions of the first nitride film 120 that form sidewalls for the gate electrodes 116. This feature has been included in independent claims 1, 6, 11 and 18 to emphasize that the first nitride film serves as an etching stopper, while the second nitride film serves as a barrier layer for blocking impurities from traveling from the interlayer insulating film to the substrate. Lee et al., on the other hand, utilizes a second nitride layer 119 that serves as an etching stopper, and that does not serve as a barrier layer with respect to an interlayer insulating film 120. Also, as clearly seen in Figure 5 of Lee et al., his second nitride layer 119 remains on the sidewalls of his gate electrodes 108, in direct contact with his first nitride layer 112a that serves as the sidewalls for the gate electrodes 108.

Therefore, all of the presently pending independent claims are patentable over the teachings of Lee et al.

With respect to dependent claims 3, 8, 13 and 22, Applicants strongly disagree with the Examiner's assertions about the thickness of the second nitride film being a matter of design choice. Rather, as explained on page 26, lines 3-9 of the specification, the thickness of the second nitride film is thin enough so as to pass the forming gas used in a final annealing step, so as not to impair the recovery of an interfacial layer. Also, the thickness of the second nitride film is thick enough so as to act as a barrier layer to prevent impurities from an interlayer insulating film from being diffused into the semiconductor substrate when the substrate is annealed in water vapor, as explained on page 25, lines 18-25 of the specification. Thus, it is not an obvious design choice for the thickness of the second nitride film, but an inventive concept that takes many different things into consideration, based on the multiple purposes of the second nitride film that heretofore were not contemplated for such a layer.

Accordingly, dependent claims 3, 8, 13 and 22 are patentable for these additional reasons, beyond those given above with respect to their base claims.

New claims 25-32 have been added to recite additional features of the present invention that are not believed to be disclosed, taught or suggested by Lee et al. For example, the features of claims 25-28 are clearly not taught by Lee et al., since Lee et al.'s second nitride layer 119 remains on the sidewalls of the gate electrodes 108 even after the formation of the contact regions. Also, the features of claims 29-32, which are directed to additional steps, are not believed to be disclosed, taught or suggested by Lee et al.

Therefore, for the reasons stated above, Applicants believe that the present application is now in condition for allowance, and an early indication of allowance is earnestly solicited.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

Respectfully submitted,

November 6, 2002
Date

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Marked-Up Claims:

1. (Amended) A method of manufacturing a semiconductor device having, on a single semiconductor substrate, a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density, comprising the steps of:

forming a gate oxide film on a surface of said semiconductor substrate;

forming gate electrodes on a surface of said gate oxide film, and forming oxide films on said gate electrodes;

uniformly forming a first nitride film having a predetermined thickness on the surface with the gate electrodes formed thereon;

masking said high-density region of said semiconductor substrate, and etching said first nitride film in only said low-density region to expose said gate oxide film in gaps between said gate electrodes;

uniformly forming a second nitride film having a predetermined thickness on the surface on which said first nitride film is etched;

forming an interlayer insulating film with an impurity introduced therein on a surface of said second nitride film;

annealing an assembly formed so far in an atmosphere containing water vapor;

self-aligning said high-density region using said first nitride film positioned on sides of said gate electrodes as an etching stopper to form contact holes reaching said semiconductor substrate in said interlayer insulating film, wherein all portions of said second nitride film that are in direct contact with said first nitride film positioned on sides of said gate electrodes are removed as a result of the self-aligning step;

forming contact electrodes connected to said semiconductor substrate in said contact holes; and

annealing an assembly formed so far with a forming gas to recover an interfacial level.

6. (Amended) A method of manufacturing a semiconductor device having, on a single semiconductor substrate, a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density, comprising the steps of:

forming a gate oxide film on a surface of said semiconductor substrate;

forming gate electrodes on a surface of said gate oxide film, and forming nitride protective films on said gate electrodes;

uniformly forming a first nitride film having a predetermined thickness on the surface with the gate electrodes formed thereon;

masking said high-density region of said semiconductor substrate, and etching said first nitride film in only said low-density region to expose said gate oxide film in gaps between said gate electrodes and also to expose said nitride protective films on said gate electrodes;

uniformly forming a second nitride film having a predetermined thickness on the surface on which said first nitride film is etched;

forming an interlayer insulating film with an impurity introduced therein on a surface of said second nitride film;

annealing an assembly formed so far in an atmosphere containing water vapor;

self-aligning said high-density region using said first nitride film positioned on sides of said gate electrodes as an etching stopper to form contact holes reaching said semiconductor substrate in said interlayer insulating film, wherein all portions of said second nitride film that are in direct contact with said first nitride film positioned on sides of said gate electrodes are removed as a result of the self-aligning step;

forming contact electrodes connected to said semiconductor substrate in said contact holes; and

annealing an assembly formed so far with a forming gas to recover an interfacial level.

11. (Amended) A method of manufacturing a semiconductor device having, on a single semiconductor substrate, a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density, comprising the steps of:

forming a gate oxide film on a surface of said semiconductor substrate;

forming gate electrodes on a surface of said gate oxide film, and forming oxide films on said gate electrodes;

uniformly forming a first nitride film having a predetermined thickness on the surface with the gate electrodes formed thereon;

masking said high-density region of said semiconductor substrate, and etching said first nitride film in only said low-density region to expose said gate oxide film in gaps between said gate electrodes;

etching the exposed gate oxide film to expose said semiconductor substrate in the gaps between gate electrodes in said low-density region;

uniformly forming a second nitride film having a predetermined thickness on the surface on which said gate oxide film is etched;

forming an interlayer insulating film with an impurity introduced therein on a surface of said second nitride film;

annealing an assembly formed so far in an atmosphere containing water vapor;

self-aligning said high-density region using said first nitride film positioned on sides of said gate electrodes as an etching stopper to form contact holes reaching said semiconductor substrate in said interlayer insulating film, wherein all portions of said second nitride film that are in direct contact with said first nitride film positioned on sides of said gate electrodes are removed as a result of the self-aligning step;

forming contact electrodes connected to said semiconductor substrate in said contact holes; and

annealing an assembly formed so far with a forming gas to recover an interfacial level.

18. (Amended) A method of manufacturing a semiconductor device having, on a single semiconductor substrate, a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density, comprising the steps of:

forming a gate oxide film on a surface of said semiconductor substrate;

forming gate electrodes on a surface of said gate oxide film, and forming nitride protective films on said gate electrodes;

uniformly forming a first nitride film having a predetermined thickness on the surface with the gate electrodes formed thereon;

etching said first nitride film in only said low-density region to expose said gate oxide film in gaps between said gate electrodes and also expose said nitride protective films on said gate electrodes;

etching the exposed gate oxide film to expose said semiconductor substrate in the gaps between gate electrodes;

uniformly forming a second nitride film having a predetermined thickness on the surface on which said gate oxide film is etched;

forming an interlayer insulating film with an impurity introduced therein on a surface of said second nitride film;

annealing an assembly formed so far in an atmosphere containing water vapor;

self-aligning said high-density region using said first nitride film positioned on sides of said gate electrodes as an etching stopper to form contact holes reaching said semiconductor substrate in said interlayer insulating film, wherein all portions of said second nitride film that are in direct contact with said first

nitride film positioned on sides of said gate electrodes are removed as a result of the self-aligning step;

forming contact electrodes connected to said semiconductor substrate in said contact holes; and

annealing an assembly formed so far with a forming gas to recover an interfacial level.

25. (New) A method according to claim 1, wherein said second nitride film only remains directly beneath said interlayer insulating film after said self-aligning step is completed.

26. (New) A method according to claim 6, wherein said second nitride film only remains directly beneath said interlayer insulating film after said self-aligning step is completed.

27. (New) A method according to claim 11, wherein said second nitride film only remains directly beneath said interlayer insulating film after said self-aligning step is completed.

28. (New) A method according to claim 18, wherein said second nitride film only remains directly beneath said interlayer insulating film after said self-aligning step is completed.

29. (New) A method according to claim 1, further comprising the steps of:

a) planarizing a top surface of the interlayer insulating film;

b) forming an oxide film on the planarized top surface of the interlayer insulating film; and

c) in the high density region, masking the oxide film in a particular pattern using a fluorine-based resist.

wherein the steps a), b) and c) are performed in sequence between the step of forming the interlayer insulating film and the step of annealing in an atmosphere containing water vapor.

30. (New) A method according to claim 6, further comprising the steps of:

a) planarizing a top surface of the interlayer insulating film;

b) forming an oxide film on the planarized top surface of the interlayer insulating film; and

c) in the high density region, masking the oxide film in a particular pattern using a fluorine-based resist,

wherein the steps a), b) and c) are performed in sequence between the step of forming the interlayer insulating film and the step of annealing in an atmosphere containing water vapor.

31. (New) A method according to claim 11, further comprising the steps of:

a) planarizing a top surface of the interlayer insulating film;

b) forming an oxide film on the planarized top surface of the interlayer insulating film; and

c) in the high density region, masking the oxide film in a particular pattern using a fluorine-based resist,

wherein the steps a), b) and c) are performed in sequence between the step of forming the interlayer insulating film and the step of annealing in an atmosphere containing water vapor.

32. (New) A method according to claim 18, further comprising the steps of:

a) planarizing a top surface of the interlayer insulating film;

b) forming an oxide film on the planarized top surface of the interlayer insulating film; and

c) in the high density region, masking the oxide film in a particular pattern using a fluorine-based resist,

wherein the steps a), b) and c) are performed in sequence between the step of forming the interlayer insulating film and the step of annealing in an atmosphere containing water vapor.